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PTO/SB/21 (08-00)

Approved for use through 10/31/2002. OMB 0651-0031

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<b>TRANSMITTAL FORM</b> <i>(to be used for all correspondence after initial filing)</i>	Application Number	09/652,322	
	Filing Date	August 31, 2000	
	First Named Inventor	Shubhendu S. MUKHERJEE	
	Group Art Unit	2152	
	Examiner Name	UNKNOWN	
Total Number of Pages in This Submission	6	Attorney Docket Number	1662-27300 (P00-309)

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ENCLOSURES (check all that apply)		
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<input type="checkbox"/> Fee Attached	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences
<input type="checkbox"/> Amendment / Reply	<input type="checkbox"/> Licensing-related Papers	<input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
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<input type="checkbox"/> Affidavits/declaration(s)	<input type="checkbox"/> Petition to Convert to a Provisional Application	<input type="checkbox"/> Status Letter
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<input checked="" type="checkbox"/> Information Disclosure Statement	<input type="checkbox"/> Request for Refund	2. TWENTY-NINE (29) References; and
<input type="checkbox"/> Certified Copy of Priority Document(s)	<input type="checkbox"/> CD, Number of CD(s) _____	3. Acknowledgment postcard.
<input type="checkbox"/> Response to Missing Parts/ Incomplete Application	Remarks	
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	Jonathan M. Harris, Reg. No. 44,144 CONLEY, ROSE & TAYON, P. C.
Signature	
Date	February 20, 2001

CERTIFICATE OF MAILING	
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on this date: February 20, 2001	
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Shubhendu S. MUKHERJEE et al. §  
Serial No.: 09/652,322 §  
Filed: August 31, 2000 §  
For: Priority Rules For Reducing §  
Network Message Routing §  
Latency §

Group Art Unit: 2152  
Examiner: UNKNOWN

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INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Att'y. Docket No. 1662-27300  
Client Docket No. P00-3094  
Date: February 20, 2001

Sir:

This Information Disclosure Statement, including completed Form PTO-1449, comprises a list of pertinent art of which Applicants are aware. A copy of each publication listed on Form PTO-1449 is enclosed herewith.

Consideration of the following related co-pending applications is requested:

ATTORNEY DOCKET NO.	SERIAL NO.	FILING DATE	TITLE
1662-23700	09/653,642	08/31/00	Apparatus And Method For Interfacing A High Speed Scan-Path With Slow-Speed Test Equipment
1662-27400	09/652,703	08/31/00	Scalable Directory Based Cache Coherence Protocol
1662-27500	09/652,391	08/31/00	Scalable Efficient I/O Port Protocol
1662-27600	09/652,552	08/31/00	Efficient Translation Lookaside Buffer Miss Processing In Computer Systems With A Large Range Of Page Sizes
1662-27700	09/651,949	08/31/00	Fault Containment And Error Recovery Techniques In A Scalable Multiprocessor
1662-27800	09/652,834	08/31/00	Speculative Directory Writes in A Directory Based Cache Coherent Nonuniform Memory Access Protocol
1662-27900	09/652,314	08/31/00	Special Encoding Of Known Bad Data
1662-28000	09/652,165	08/31/00	Broadcast Invalidate Scheme

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**Serial No.:** 09/652,322  
**Filed:** August 31, 2000

ATTORNEY DOCKET NO.	SERIAL NO.	FILING DATE	TITLE
1662-28100	09/652,704	08/31/00	Mechanism To Track All Open Pages In A DRAM Memory System
1662-28200	09/653,093	08/31/00	Programmable DRAM Address Mapping Mechanism
1662-29200	09/652,323	08/31/00	Computer Architecture And System For Efficient Management Of Bi-Directional Bus
1662-29300	09/652,452	08/31/00	An Efficient Address Interleaving With Simultaneous Multiple Locality Options
1662-29400	09/653,092	08/31/00	A High Performance Way Allocation Strategy For A Multi-Way Associative Cache System
1662-29500	09/651,948	08/31/00	Method And System For Absorbing Defects In High Performance Microprocessor With A Large N-Way Set Associative Cache
1662-29600	09/652,324	08/31/00	A Method For Reducing Directory Writes And Latency In A High Performance, Directory-Based, Coherency Protocol
1662-30800	09/653,094	08/31/00	Mechanism To Reorder Memory Read And Write Transactions For Reduced Latency And Increased Bandwidth
1662-30900	09/652,325	08/31/00	System For Minimizing Memory Bank Conflicts In A Computer System
1662-31000	09/651,945	08/31/00	Computer Resource Management And Allocation System
1662-31100	09/653,643	08/31/00	Input Data Recovery Scheme
1662-31200	09/652,451	08/31/00	Fast Lane Prefetching
1662-31300	09/652,480	08/31/00	Mechanism For Synchronizing Multiple Skewed Source-Synchronous Data Channels With Automatic Initialization Feature
1662-31400	09/651,924	08/31/00	Mechanism To Control The Allocation Of An N-Source Shared Buffer
1662-31500	09/652,315	08/31/00	Chaining Directory Reads And Writes To Reduce DRAM Bandwidth In A Directory Based CC-NUMA Protocol

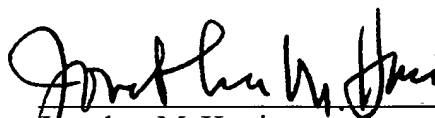
The submission of this Information Disclosure Statement and the references submitted therewith is not an admission that the art cited is "prior" with respect to the present invention, nor is it a representation, that no better art exists. Applicants hereby reserve the right to swear behind

**Serial No.:** 09/652,322  
**Filed:** August 31, 2000

or otherwise disprove any alleged "prior" nature of any art cited should the facts support and the situation warrant such an action. It is submitted that the art cited does not constitute a bar to the patentability of Applicants' invention under 35 U.S.C. § 102 or § 103.

No Office Action has been received in the present application. Nonetheless, in the event that an Office Action dated prior to the mailing date of this Information Disclosure Statement has been issued, please charge Deposit Account 03-2769, Conley, Rose & Tayon, P.C., in the amount of \$180, so that this Information Disclosure Statement may be considered under Rule 1.97(c). A duplicate of this Information Disclosure Statement is attached for that purpose.

Respectfully submitted,



Jonathan M. Harris  
PTO Reg. No. 44,144  
CONLEY, ROSE & TAYON  
P.O. Box 3267  
Houston, TX 77253-3267  
(713) 238-8000 (Phone)  
(713) 238-8008 (Fax)

ATTORNEY FOR APPLICANTS